

### IN THE SPECIFICATION

Please amend the paragraphs of the specification with the replacement paragraphs as indicated below.

Please amend the group of paragraphs beginning on page 2, line 19 through page 5 line 5 as shown below.

FIG. 1 is a block diagram of a processing system in accordance with some embodiments of the present invention. Processing system 100 may be part of almost any computing or processing system including computer systems, server systems, and wireless communication devices and systems. In some embodiments, system 100 may be part of a pipelined system. System 100 comprises bus arbiter 102 which receives requests 116 from a plurality of requestors [[106]] (i.e., requesting devices), shown generally as requestors 106A, 106B and 106C, requesting use of shared resource 108.

Requestors 106A, 106B and 106C may include any device or element that requests use of a shared resource. Examples of requestors 106A, 106B and 106C may include, for example, memory controllers, ~~such as memory controller (MC)~~ 104, processors and processing resources including cryptographic processors, direct memory access (DMA) units, network interfaces, digital signal processors (DSPs), network controllers including wireless local area network controllers, signal processors, floating-point units (FPUs), application accelerators, and/or data acquisition devices. In some embodiments, memory controller (MC) 104 may function as a requestor, such as requestors 106A, 106B and 106C.

Requestors 106A, 106B and 106C generate bus requests 116 for bus arbiter 102 and may receive bus grants 118 from bus arbiter 102. Bus arbiter 102 may provide a bus grant for a request to a requestor in accordance with one or more arbitration schemes, including, for example, priority based arbitration

schemes or fixed arbitration schemes. In some embodiments, bus requests 116 and bus grants 118 may be communicated between arbiter 102 and requestors over a grant/request bus (not illustrated).

When granted access, one or more of requestors 106A, 106B and 106C may access one or more of shared resources 108 over system bus 114. Shared resource 108 may include one or more resources that may be shared among requestors 106A, 106B and 106C. Shared resource 108, may include a processor, a central processing unit, a particularly-configured processing engine (e.g., for cryptographic processing), or other resource that may be shared by one or more of requestors 106A, 106B and 106C over bus 114. Bus 114 may be almost any type of data bus that supports multiple clients using some form of arbitration. In some embodiments, bus 114 may be a 32-bit or 64-bit bus including a PCI bus, a PCI-express (PCIX) bus or a third-generation input/output (3GIO) bus, although the scope of the invention is not limited in this respect.

In accordance with some embodiments, bus arbiter 102 generates bus-activity indicator (BAI) 120 for use by one or more of requestors 106A, 106B and 106C. Bus-activity indicator 120 may be an indication of how busy system bus 114 has been during a recent system-bus observation window. The system-bus observation window may comprise a prior predetermined number of system-bus cycles. One or more of requestors may predict when to generate a bus request based on bus-activity indicator 120, a bus-usage efficiency indicator and a bus-bandwidth usage indicator. The bus-usage efficiency indicator may be generated by one of requestors 106A, 106B and 106C based on a number of unused bus cycles that were granted to the requestor during a prior observation window. The bus-bandwidth usage indicator may be generated by the requestor based on a number of bus transactions effectively utilized by the requestor during the prior observation window.

In some embodiments, when bus-activity indicator 120 indicates that system bus 114 is not busy, a requestor, such as one of requestors 106A, 106B and 106C, may engage in full speculation generating a bus request ahead-of-time,

which may be a maximum predetermined number of bus cycles ahead-of-time. When bus-activity indicator 120 indicates that the system bus is busy, the requestor may predict how early to generate the bus request based on the bus-activity indicator, the bus-usage efficiency indicator and the bus-bandwidth usage indicator.

In some embodiments, a requestor, such as one of requestors 106A, 106B and 106C, may predict when to generate the bus request based on one of a plurality of speculation states, which may be at least initially determined by bus-activity indicator 120. In these embodiments, the requestor may transition among the various speculation states based on the bus-usage efficiency indicator and the bus-bandwidth usage indicator. In some embodiments, the requestor may transition among the various speculation states based on changes in the bus-usage efficiency indicator and/or bus-bandwidth usage indicator. In some embodiments, the requestor may determine a number of bus cycles to generate the bus request ahead-of-time based on an imminence level of a transaction for which the bus request is to be generated.

In some embodiments, bus-activity indicator 120 may comprises a two-bit value broadcasted by bus arbiter 102 to one or more of requestors 106A, 106B and 106C. The two-bit value may be broadcasted over a two-wireline connection to one or more of requestors 106A, 106B and 106C, although the scope of the invention is not limited in this respect.

In wireless embodiments, system 100 may include wireless network interface 110, such as a network interface card (NIC). In these embodiments, wireless network interface 110 may operate as a requestor, such as one of requestors 106A, 106B and 106C, and may communicate RF signals with other networked devices, such as an access point, using antenna 112. In these embodiments, system 100, including wireless network interface 110 and antenna 112, may be part of a wireless communication device, such as a personal digital assistant (PDA), a laptop or portable computer with wireless communication capability, a web tablet, a wireless telephone, a wireless headset, a pager, an

instant messaging device, an MP3 player, a digital camera, an access point, or other device that may receive and/or transmit information wirelessly. In these embodiments, wireless network interface 110 may receive RF communications in accordance with specific communication standards, such as the IEEE 802.11(a), 802.11(b) and/or 802.11(g) standards for wireless local area network standards, although wireless network interface 110 may receive communications in accordance with other techniques including Digital Video Broadcasting Terrestrial (DVB-T) broadcasting standard, and the High performance radio Local Area Network (HiperLAN) standard. Antenna 112 may be almost any type of antenna including a dipole antenna, a monopole antenna, a loop antenna, a microstrip antenna or other type of antenna suitable for reception and/or transmission of RF signals, which may be processed by wireless network interface 110.

Please amend the paragraph beginning on page 5, line 22 as shown below.

FIG. 2 is a block diagram of a requestor in accordance with some embodiments of the present invention. Requestor 200 may be suitable for use as one of requestors 106A, 106B and 106C (FIG. 1) although other requestors may also be suitable. Requestor 200 comprises logic circuitry 202 to generate a bus-usage efficiency indicator and a bus-bandwidth usage indicator, and logic circuitry 204 to predict when to generate a bus request based on the bus-usage efficiency indicator and the bus-bandwidth usage indicator. Requestor 200 may also include other system elements 208 to allow requestor 200 to serve its primary purpose (e.g., as a memory controller or memory-control unit (MCU), a processor or processing resource, a direct memory access (DMA) unit, or a network interface). Requestor 200 may also include one or more internal communications paths 210 and/or 212 too provide internal communications between elements, as well as communications with external elements, such as a system bus.

Please amend the paragraph beginning on page 7, line 21 as shown below.

FIG. 3 is state diagram in accordance with some embodiments of the present invention. State diagram 300 illustrates speculation states 302, 304 and 306 in which a requestor, such as one of requestors 106A, 106B and 106C (FIG. 1) may be in when predicting when to generate a bus request. The speculation state may be initially set or determined based on a bus-activity indicator, such as BAI 120 (FIG. 1), received from a bus arbiter. The speculation states may include full-speculation state 302, delayed-speculation state 304 and no-speculation state 306.

Please amend the paragraph beginning on page 10, line 22 as shown below.

In some embodiments, a requestor may further determine a number of bus cycles to generate the bus request ahead-of-time based on an imminence level of a transaction for which the bus request is to be generated. In these embodiments, an imminence bit may be set. In some embodiments, memory controller 104 (FIG. 1), as one of requestors 106A, 106B and 106C (FIG. 1), may be coupled to various memories 105 (FIG. 1), which may include off-chip memory. Memory controller 104 (FIG. 1) may make an independent decision on whether there is need to request use of bus 114 (FIG. 1) to service an outstanding transaction, and may base this decision on whether the transaction is considered imminent. Transactions may be considered imminent when they reach a predetermined state of completion. In some embodiments, a requestor, such as memory controller 104 (FIG. 1), may determine the existence of a need for a bus request and may proceed to implement the request in accordance with the speculation state.

Please amend the paragraph beginning on page 11, line 20 as shown below.

FIG. 4 is a procedure for predicting when to generate a bus request in accordance with some embodiments of the present invention. Procedure 400 may be performed by a requestor, such as one of requestors 106A, 106B and 106C (FIG. 1) although other system elements may also perform procedure 400.

Please amend the paragraph beginning on page 11, line 24 as shown below.

In operation 402, a bus-activity indicator, such as bus-activity indicator 120 (FIG. 1), is received from a bus arbiter. The bus arbiter may generate the bus-activity indicator based on system bus activity and may be broadcast to one or more of requestors 106A, 106B and 106C (FIG. 1). In some embodiments, the bus-activity indicator may indicate whether the system bus is busy or idle.

Please amend the paragraph beginning on page 11, line 29 as shown below.

In operation 404, a requestor may enter an initial speculation state, such as full-speculation state 302 (FIG. 3). Operation 406 determines when the bus-activity indicator indicates that the system bus has been busy during a prior observation window. When operation 406 determines that the system bus is not busy, or idle, operation ~~[[402]]~~ 404 is repeated and the requestor may remain in the full-speculation state. When operation 406 determines that the system bus is busy, operation 408 is performed.